REMARKS

I. Double Patenting Rejections

Claims 1 and 8 were provisionally rejected under the judicially-created doctrine of obviousness-type double patenting over Claims 1 and 18 of copending U.S. patent application number 09/877,719. In response to this rejection, Applicants submit herewith the appropriate terminal disclaimer and fee. In view of these submissions, Applicants respectfully request withdrawal of the obviousness-type double patenting rejections.

II. Amendment to the Specification

Applicants have amended the specification to include a missing serial number for a copending patent application.

III. Objections to the Claims

The dependent claims were objected to for using the language "the invention of." In response to these objections, Applicants have amended the claims as suggested in the Office Action. However, because Claims 15 and 16 multiply depend from both method Claims 1 and 12 and memory device Claim 8, Applicants have amended Claims 15 and 16 so they only depend on the method claims and have added new Claims 17 and 18, which depend from memory device Claim 8. In view of these amendments, Applicants respectfully submit that the objections to the claims have been overcome.

IV. Claim Rejections Under 35 U.S.C. § 112, Second Paragraph

Claim 1 was rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for the lack of antecedent basis of the term "the memory array," since the term "a write-once memory array" was earlier recited. Claims 2-7 were also rejected as depending from Claim 1 and containing the same deficiency. In response to these rejections, Applicants have amended Claim

1 and several others of the pending claims to add the phrase "write-once" in front of the phrase "memory array." In view of these amendments, Applicants respectfully submit that the 35 U.S.C. § 112, second paragraph, rejections have been overcome.

V. Claim Rejections Under 35 U.S.C. § 103(a)

Independent Claims 1, 8, and 12 each recite elements relating to an inverting bits. These claims were rejected under 35 U.S.C. § 103(a) as being unpatentable over the proposed combination of U.S. Patent No. 6,377,526 to Vining et al. and U.S. Patent No. 6,490,703 to de la Iglesia et al. In the Office Action, it was admitted that Vining et al. fails to teach these elements, and de la Iglesia et al. was relied upon in an attempt to cure this deficiency. Applicants respectfully request reconsideration and withdrawal of these rejections in view of the amendments made to the independent claims. Before turning to the claims, Applicants present a brief overview of de la Iglesia et al.

De la Iglesia et al. is directed to a bus power savings technique in which bits in a data string are inverted when the number of logic one bits in the data string exceeds fifty percent of the total number of bits. This technique is described, *inter alia*, at col. 2, line 65 – col. 3, line 2 (emphasis added):

> In a preferred embodiment, the invention saves power in systems where power consumption is high during a logic one state by inverting the data signal ***when the number of bits at the logic one state in that data signal exceed [sic] fifty percent of the total number of bits***.

Because storing logic one bits requires more power that storing logic zero bits, inverting the bits when the majority of bits are logic one bits saves power. When the minority of bits are logic one bits, the bits are not inverted, since inverting the bits in that situation would result in more logic one bits and, hence, higher power consumption.

Turning now to the claims, independent Claim 1 has been amended to recite that the inverting takes place ***irrespective of a number of logic one bits in the plurality of bits***. Support for this amendment can be found on page 12, lines 13-15, where it is discussed that inverting bits essentially redefines the value of the unwritten bit in the memory array. To "essentially redefine" the value of the unwritten bit in the memory array, the inverting of bits is irrespective of the number of logic one bits; otherwise, the value of the unwritten bit would not be "essentially redefined" since some plurality of bits would be stored in an inverted form while others would be stored in a non-inverted form. Additional support for this amendment can be found in the example set forth in Figures 16A and 17A, where the data string 0000 is inverted even though the number of logic one bits (zero) does not exceed fifty percent of the total number of bits (four).

Applicants have amended independent Claims 8 and 12 similar to Claim 1. In independent Claim 8, Applicants have specified that the controller is operative to invert the plurality of bits irrespective of a number of logic one bits in the plurality of bits. In independent Claim 12, Applicants have specified that the bits are stored in an inverted form irrespective of a number of logic one bits in the plurality of bits. Further, Applicants have added new Claims 19-21, which depend from independent Claims 1, 8, and 12, respectively, and specify that the plurality of bits are inverted even when a number of logic one bits in the plurality of bits does not exceed fifty percent of a total number of bits in the plurality of bits.

Turning now to the proposed combination, even if the motivation to combine Vining et al. with de la Iglesia et al. is proper,[1] the proposed combination does not yield each and every element of the independent claims — the independent claims require the inverting to take place

[1] Applicants reserve the right to present arguments at a later time regarding why one skilled in the art would not have been motivated to combine Vining et al. and de la Iglesia et al.

irrespective of the number of logic one bits, while the inverting in the proposed combination is ***dependent upon*** the number of logic one bits of bits. Applicants also submit that one skilled in the art would not have been motivated to further modify the proposed combination to yield the elements added to the independent claims because such a modification would be contrary to the basic operating principle in de la Iglesia et al. If de la Iglesia et al. were modified such that a data string is inverted irrespective of the number of logic one bits, some data strings would be stored with more logic one bits than logic zero bits. This would result in higher power consumption, thereby reintroducing the very problem that de la Iglesia et al. seeks to overcome.

Because the proposed combination does not teach the elements added to the independent claims in this amendment, Applicants respectfully request removal of the rejections of independent Claims 1, 8, and 12 and their dependent claims.[2]

VI. Conclusion

In view of the above amendments and remarks, Applicants respectfully submit that this application is in condition for allowance. Reconsideration is respectfully requested. If there are any questions concerning this Amendment, the Examiner is invited to contact the undersigned attorney at (312) 321-4719.

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Respectfully submitted,

BRINKS HOFER GILSON & LIONE
P.O. Box 10395
Chicago, Illinois 60610
(312) 321-4719

Joseph F. Hetz
Reg. No. 41,070
Attorney for Applicants

[2] The dependent claims present additional grounds of patentability over the cited references. Applicants reserve the right to argue these additional grounds at a later time, if necessary.